DAUGHTERCARD-BASED SYSTEM SOFTWARE AND HARDWARE FUNCTIONALITY-DEFINING MECHANISM

FIELD OF THE INVENTION

[0001] The present invention relates in general to electronic systems and subsystems therefor, such as but not limited to test apparatus for telecommunication equipment and components thereof, and is particularly directed to a mechanism for establishing both the software and hardware functionality of processor-controlled signal processing apparatus, in response to the presence of a daughtercard which contains such functionality, and imparts the same to the signal processing system's supervisory motherboard. In the absence of such a daughtercard, the motherboard executes a resident default operation control mechanism, so as to cause the equipment to exhibit the default hardware functionality of the base system. If a daughtercard is present, however, the motherboard executes whatever replacement operation control software is provided on the daughtercard - causing the signal processing

equipment to acquire a hardware functionality exclusive of the motherboard default.

BACKGROUND OF THE INVENTION

[0002] Processor-controlled electronic systems are customarily provided with auxiliary card slots, that allow a user to augment the functionality of a base system with the installation of one or more daughtercards. Non-limiting examples include additional memory, printer cards, fax/modem cards, graphics accelerator cards, game cards, and the like. Now although these components serve to enhance or expand the original computer system with one or more additional operational or application features, they do not, nor are they intended to, effectively modify the hardware functionality of the base system. The base information processing system still performs all of its previous functions. Where modification of the hardware functionality of the base processing system is desired, it is customary practice to provide an upgrade of the base system software installed on the motherboard, coupled with installation, or replacement, of whatever hardware is associated with the new software. It goes without saying that such a conventional approach to system modification is undesirably labor-intensive, time-consuming and costly.

SUMMARY OF THE INVENTION

[0003] In accordance with the present invention, shortcomings of conventional schemes for upgrading the hardware and software of a conventional processor-controlled electronic utility (e.g., information signal processing) system, such as those described above, are effectively obviated by causing the overall operation and hardware functionality of an upgraded or modified base system to be daughtercard-dependent. Namely, if a daughtercard is present, the motherboard will execute whatever replacement operation control software is provided on the daughtercard - causing the signal processing equipment to acquire a hardware functionality different from the motherboard-based default.

[0004] For this purpose, as in a conventional system, the base system's motherboard includes a system-controlling microprocessor, boot flash memory, application flash memory containing default system functionality firmware, and a daughtercard detector logic circuit. When the base system is turned on, or reset, it boots up by executing the software in the boot flash memory. Whether it is to execute the default application firmware stored in its application flash memory or separate and distinct firmware contain in flash memory on the daughtercard depends upon whether the daughtercard detector logic circuit has detected the presence of a daughtercard.

[0005] Pursuant to the invention, the daughtercard has its own application flash memory containing operational

firmware associated with on-board hardware such as a digital communication transceiver. The functionality of the application firmware in the daughtercard's flash memory is based upon and is effective to control operation of both the daughtercard's on-board hardware as well as the overall operation of the motherboard in the course of executing the daughtercard's firmware. Namely, the daughtercard-resident firmware is intended to be executed by the motherboard processor 'in place of' the base system application firmware contained the default flash memory of the motherboard. This exclusive execution of daughtercard firmware is in direct contrast to a conventional system which continues to perform all of its previous functions when a daughtercard has been added.

[0006] In order to detect the presence of a daughtercard, the communication bus that links the motherboard to a daughtercard receptacle includes an application firmware control link signal that represents which application flash memory is to be accessed by the motherboard's processor. In the absence of insertion of a daughtercard, this control link is normally relatively weakly held at a high by a pull-up resistor coupled to a high logic level voltage rail. In this state motherboard's processor is steered to the default firmware within its own application flash memory. On the other hand, if a daughtercard has been inserted into the daughtercard receptacle, the daughtercard termination of the control link is grounded, which pulls the control

link to a logical low. For this state the daughtercard detector logic circuit steers the motherboard's processor to the application firmware within daughtercard-resident flash memory.

[0007] Advantageously, because the application firmware stored in the daughtercard's flash memory is intimately related with and serves to control operation of the daughtercard's on-board hardware, and it is the daughtercard that defines the overall hardware and software complexion of the base system motherboard, no modification of either the hardware or the software of the motherboard is required.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The single Figure diagrammatically illustrates a processor-based utility electronic utility control system employing a daughtercard-based software and hardware modification mechanism in accordance with the present invention.

DETAILED DESCRIPTION

[0009] Before describing the daughtercard-based system software and hardware functionality control mechanism in accordance with the present invention, it should be observed that the invention effectively resides primarily in a modular arrangement of conventional digital communication and signal processing circuits and components and associated software therefor. In a practical implementation that facilitates their being

packaged in a hardware-efficient equipment configuration, this modular arrangement may be readily implemented as field programmable gate array (FPGA), or application specific integrated circuit (ASIC) chip sets. Consequently, the configuration of such arrangement of circuits and components and the manner in which they are interfaced with other equipment have, for the most part, been illustrated in the drawings by a readily understandable block diagram, which shows only those specific details that are pertinent to the present invention, so as not to obscure the disclosure with details which will be readily apparent to those skilled in the art having the benefit of the description herein. The block diagram illustration is primarily intended to show the major components of the invention in a convenient functional grouping, whereby the present invention may be more readily understood.

[00010] Attention is now directed to the single Figure, wherein an embodiment of the present invention is diagrammatically illustrated as comprising an electronic control system motherboard 10 installed in a base equipment support housing, identified by broken lines 11. As is common practice in processor-controlled electronic utility application systems, the motherboard contains a microprocessor 12, a boot flash memory 13 containing boot code, an application flash memory 14 containing default system functionality firmware, and a daughtercard detector logic circuit 15. As will be described, this latter circuit preferably comprises an

address decode chip, that is operative to controllably generate a pair signals NFLASH_CSL and NFLASH_CSH for selecting flash memories on the motherboard. It is also operative to controllably generate a pair signals DFLASH_CSL and DFLASH_CSH for selecting flash memories on the daughtercard.

[00011] Whenever the base system is turned on, or reset, it boots up by executing the software in local flash memory 13. Whether it is to execute the default application firmware stored in flash memory 14 or separate and distinct firmware contain in flash memory on the daughtercard depends upon whether the daughtercard detector logic circuit 15 has detected the presence of a daughtercard. To detect the presence of a daughtercard, the logic circuit 15 is preferably programmed at manufacture with a prescribed set of control code, such as that set forth below.

[00012] More particularly, the motherboard 10 is provided with a standard daughtercard receptacle 16 that is configured to receive and be engaged by a corresponding card insertion element or terminal edge connector 26 mounted on a daughtercard 20. As pointed out briefly above, the daughtercard contains its own application flash memory 23, which contains operational firmware associated with on-board hardware 24, such as a prescribed communication transceiver interface (e.g. a DS3 communication interface, Ethernet interface, and the like). The application firmware contained in the flash memory 23 on the daughtercard is based upon and is

effective to control operation of the daughtercard's on-board transceiver (hardware) 24, as well as the overall operation of the motherboard in executing the functionality of the daughtercard's firmware. Namely, the daughtercard-resident firmware is intended to be executed by the motherboard processor 12 'in place of' the base system application firmware contained the default flash memory 14 of the motherboard. (As described above, This is in contrast to a conventional system which, continues to perform all of its previous functions when a daughtercard has been added.)

[00013] For this purpose, the communication bus 30 that traverses the terminal connector 26 on the daughtercard and the daughtercard insertion receptacle 16 on the motherboard 10 includes an application firmware control link 31, as well as a flash memory communication bus 32 coupled to both the motherboard's application firmware flash memory 14 and the daughtercard's application firmware flash memory 23. The firmware control link 31 provides a signal D_ID that represents which application flash memory is to be employed by the motherboard's processor. As described briefly above, in the absence of insertion of a daughtercard, control link 31 is normally pulled high (e.g., the D_ID signal is a logical '1') by a pull-up resistor 33 coupled to Vdd. In this state the daughtercard detector logic circuit 15 steers the processor 12 to the default firmware within the flash memory 14. However, if a daughtercard has been inserted into the daughtercard receptacle 16, the daughtercard

termination 34 of the control link 31, which is coupled to ground, will pull the control link low (e.g., the D_ID signal is a logical '0'). For this state the daughtercard detector logic circuit 15 steers the processor 12 over link 32 to the application firmware within daughtercard-resident flash memory 23.

[00014] For purposes of providing a non-limiting example, the daughtercard detector logic circuit 15 may be programmed with the following control code:

[00015] Normal Program Flash Memory (4M) base card

```
    nFLASHCSL <- '0' when (nCS(3) = '0' and A21 = '0'
and D_ID = '1') else '1';
--Normal Access High 2MB base card
    nFLASHCSH <- '0' when (nCS(3) = '0' and A21 = '1'
and D_ID = '1') else '1';
--Normal Access High 2MB base card (optional)
```

[00016] Normal Program Flash Memory (4M) daughter card

```
    nDFLASH_CSL <- '0' when (nCS(3) = '0' and A21 = '0'
and D_ID = '0') else '1';
--Normal Access Low 2MB daughter
    nDFLASH_CSH <- '0' when (nCS(3) = '0' and A21 = '1'
and D_ID = '0') else '1';
--Normal Access High 2MB daughter (optional)
```

[00017] Because the application firmware stored in flash memory 23 is intimately related with and serves to control operation of the daughtercard's on-board

hardware (e.g., transceiver 24), and the control processor 12 on board the motherboard derives its control functionality exclusively from the daughtercard, no modification of either hardware or software of the motherboard is required. Where the daughtercard contains a digital communication interface, such as one of those referenced above, that interface is coupled via external ports to an associated communication link for transporting corresponding communication signals with respective a source/destination therefor.

[00018] While we have shown and described an embodiment in accordance with the present invention, it is to be understood that the same is not limited thereto but is susceptible to numerous changes and modifications as known to a person skilled in the art, and we therefore do not wish to be limited to the details shown and described herein, but intend to cover all such changes and modifications as are obvious to one of ordinary skill in the art.